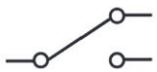
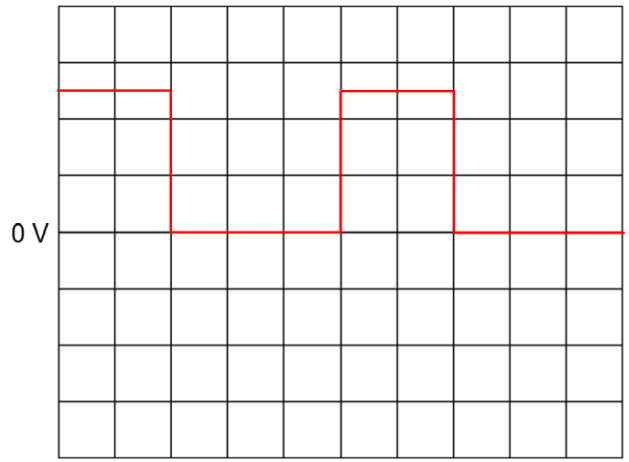
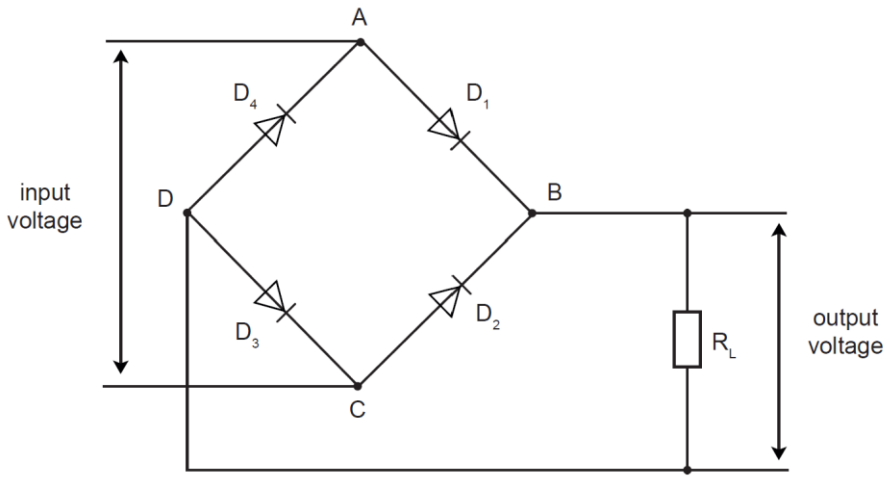
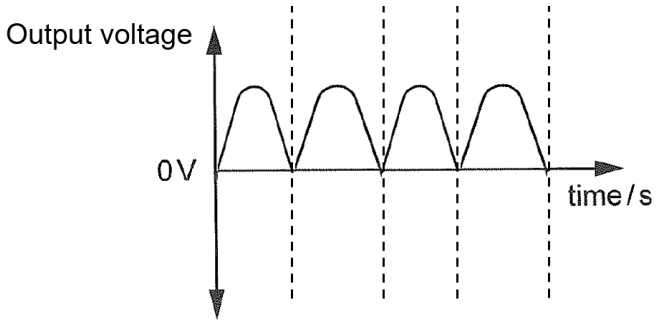
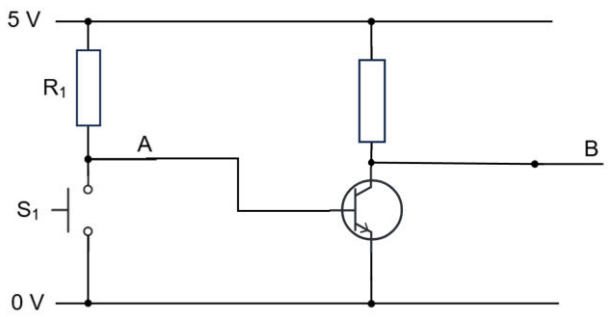
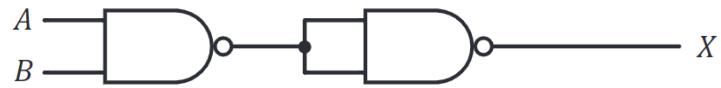
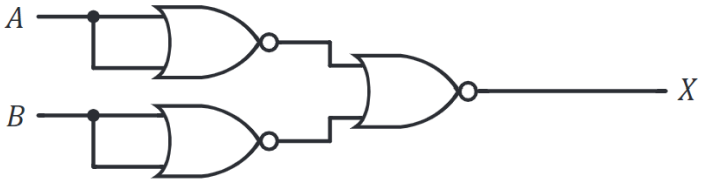
School of Science and Technology, Singapore
Preliminary Examination 2024
Electronics

Mark Scheme

Qn		Answer	Mark Scheme	Marker's Comments
1			B1 each	
				
		Zener diode		
		PNP bipolar junction transistor	Accept PNP BJT or PNP transistor	
		AC source		
2	**(a)**	Violet, green, black, gold	B2 4 bands correct B1 3 bands correct	
	(b)	$P = I^2R = (80 \times 10^{-3})^2 \times 75$ $= 0.48$ W	M1 A1	
	(c)	1 W (more than twice the maximum power)	B1	
3	**(a)**	$I_1 = 2$ mA $I_2 = 10$ mA $I_3 = 13$ mA	B1 B1 B1	
	(b)	$V_1 = 1.6$ V $V_2 = 2.9$ V	B1 each	

4	**(a)**		B1 for period B1 for voltage levels B1 for duty cycle No mark if waveform is not rectangular.	
	(b)	The signal repeats itself at regularly intervals.	B1	
5	**(a)**	4700 pF	B1	
	(b)	Capacitor A is non-polarised while capacitor B is polarised.	B1	
6	**(a)**		B2 All diodes correct positions and direction B1 two diodes correct positions and direction No mark if symbol is wrong.	

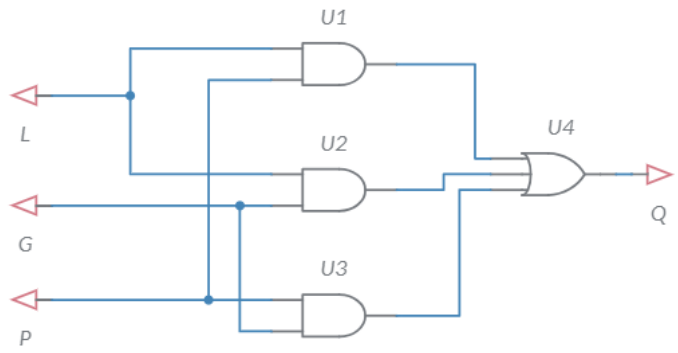
	(b)	Diodes allow currents to pass through in one direction only.	B1	
	(c)		• B2 for all 4 halves correct • B1 for 2 or 3 halves correct	
7	**(a)**	HIGH LOW	B1 for both correct	
	(b)	R_1 connects point A to 5 V when S_1 is open. This prevents point A from floating when S_1 is open. <u>Alternative answer</u>: R_1 provides a resistance between 5 V and 0 V. This prevents a short circuit between 5 V and 0V when the switch is closed.	B1 B1 B1 B1	
	(c)		B1 Point A to base B1 Collector to point B and to 5 V through resistor B1 Emitter to ground	

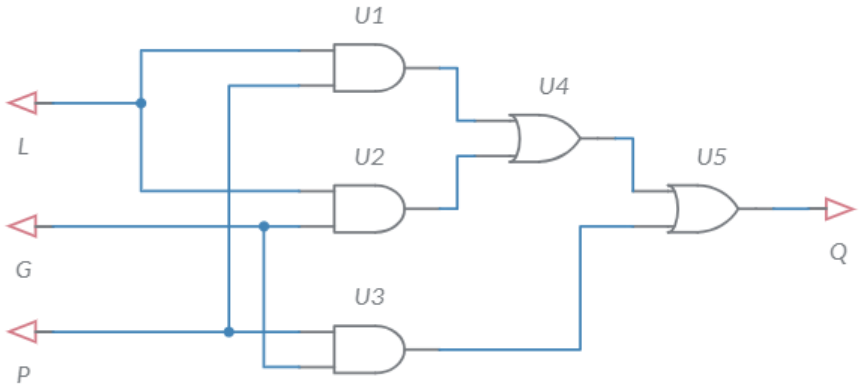
8	**(a)**	A universal gate is a logic gate that can be used to implement all other types of logic gates.		B1	
	(b)	**(i)**		B1	
		(ii)		B2 All correct B1 Only invert both inputs	
9	**(a)**	0001 0100		B1	
	(b)	1110		B1	
	(c)	Advantage: Ready / easy to be used for decimal display Disadvantage: more bits to represent the number / needs more memory to store		B1 B1	
10	**(a)**	Pin 2 causes output to go HIGH when the voltage at the pin goes below 1/3 of Vcc Pin 6 causes output to go LOW when the voltage at the pin goes above 2/3 of Vcc		B1 B1 B1 B1	
	(b)	$T = \frac{(R_1+2R_2)C}{1.44}$; $T = \frac{(5.6\times10^3 + 2\times33\times10^3)10\times10^{-6}}{1.44}$ = 0.50 Hz		M1 A1	
	(c)	C1 charges through both R1 and R2, but discharges through R2 only.		B1	
	(d)	Q = C × V; = 10 μF × 4.0 V = 40 μC		M1 A1	

<table>
<tr><td></td><td>(e)</td><td>The period will increase.
When two capacitors are connected in parallel, the effective capacitance increases.
C1 will take longer to charge and discharge.</td><td>B1
B1

B1</td><td></td></tr>
<tr><td></td><td>(f)</td><td>Voltage across R_3 = 8.1 – 2.0 = 6.1 V
R_3, $R = \frac{V}{I} = \frac{6.1}{20\times10^{-3}}$ = 305 Ω
Choose 330 Ω (Accept 300 Ω)</td><td>M1
M1

A1</td><td></td></tr>
<tr><td>11</td><td>(a)</td><td>
<table>
<tr><th>G</th><th>L</th><th>P</th><th>Q</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
</td><td>B3 All rows correct
B2 6 or 7 rows correct
B1 4 or 5 rows correct</td><td></td></tr>
<tr><td></td><td>(b)</td><td>Q = $\bar{G}\cdot L\cdot P + G\cdot\bar{L}\cdot P + G\cdot L\cdot\bar{P} + G\cdot L\cdot P$</td><td>B1</td><td></td></tr>
<tr><td></td><td>(c)</td><td>
<table>
<tr><th>G \ LP</th><th>00</th><th>01</th><th>11</th><th>10</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
</table>
</td><td>B3 All loops correct
B2 Two loops correct
B1 One loop correct</td><td></td></tr>
<tr><td></td><td>(d)</td><td>Q = $L\cdot P + G\cdot P + G\cdot L$</td><td>B1</td><td></td></tr>
</table>

<table>
<tr>
<td></td>
<td>(e)</td>
<td colspan="2"> 

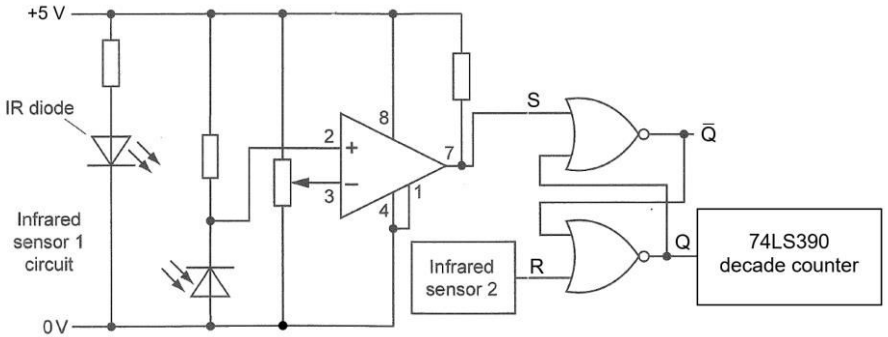
Or

</td>
<td>B3 All AND terms correct & ORed

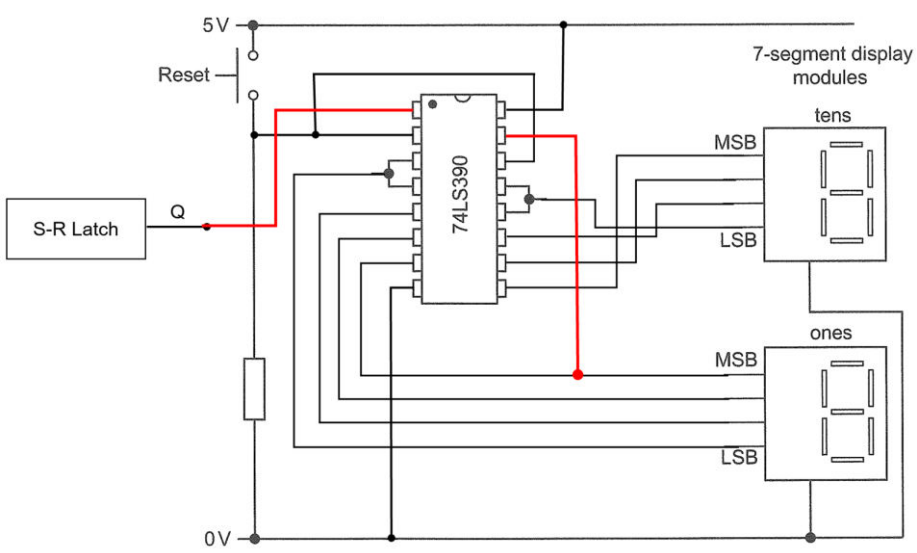
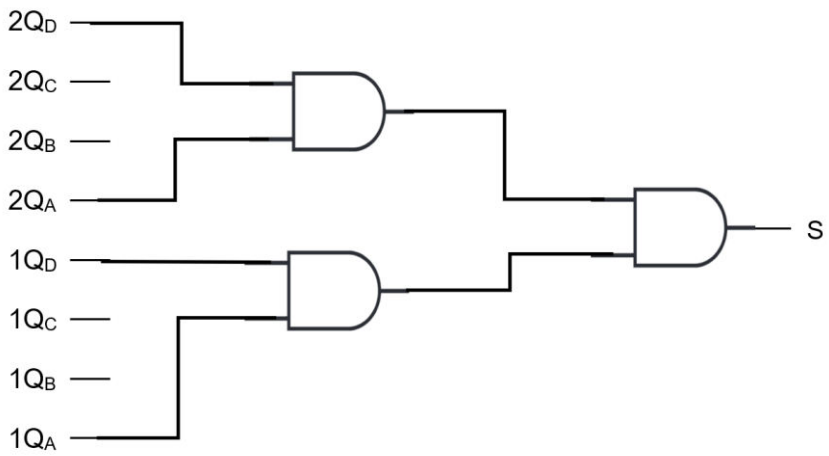
B2 Two AND terms correct & ORed

B1 One AND term correct</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(f)</td>
<td>(i)</td>
<td>
<table>
<tr><th>Pin number</th><th>Function</th></tr>
<tr><td>14</td><td>Connects to the power supply</td></tr>
<tr><td>6</td><td>Gate B output</td></tr>
</table>
</td>
<td>B1 each</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(ii)</td>
<td>Integrated circuit</td>
<td>B1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(iii)</td>
<td>It means that the IC will treat an <u>input voltage of 2.0 V or higher as logic 1 or HGH.</u></td>
<td>B1</td>
<td></td>
</tr>
</table>

12	**(a)**	To adjust the sensitivity of the circuit. or To adjust the potential difference across A.		B1	
	(b)	**(i)**	65% of 50k = 32.5k or 33 k Voltage at A = (32.5 k/(32.5k+30k)) *6.0V or (33k/ (33k+30k)) *6.0V = 3.1 V (2.s.f) or 3.1 V	 M1 A1	
		(ii)	Voltage at A = 3.1 V $3.1\ V - I_B R_B - V_{BE} - V_{BE} = 0$ $3.1\ V - I_B R_B - 1.4\ V = 0$ $I_B R_B = 1.7\ V$ $R_B = 1.7\ V / 100\ \mu A$ $= 17\ k\Omega$	 M1 A1	
	(c)	Voltage reading <u>decreases</u>. Temperature increases, the <u>resistance across the thermistor decreases</u>, causing the voltage across to decrease.		B1 B1	
	(d)	$I_C = \beta_{dc} \times I_B$ $= 300 \times 100\ \mu A$ $= 30\ mA$ <u>30 mA is lower than 350 mA</u> of the rated current of the lamp, hence unable to drive the load at rated current.		M1 A1	
	(e)	**(i)**	Darlington Pair	B1	
		(ii)	$6.0 - I_{C(sat)}\ 17 - 0.9\ V = 0$ $I_{C(sat)} = (6-0.9)/17$ = 300 mA (2 s.f)	M1 A1	

<table>
<tr><td></td><td></td><td>(iii)</td><td>$I_{B(sat)} = I_{c(sat)} / (\beta_{dc1} \times \beta_{dc2})$
$= 300\ mA / (300 \times 40)$
$= 25\ \mu A$ (2 s.f)</td><td>M1

A1</td><td></td></tr>
<tr><td></td><td></td><td>(iv)</td><td><u>Increase Vcc/ power supply</u> to 6.9 V to compensate for the $V_{CE(sat)}$.</td><td>B1</td><td></td></tr>
<tr><td>13</td><td>(a)</td><td colspan="2">Only allows current to pass through when reversed-biased
if IR falls on it.</td><td>B1
B1</td><td></td></tr>
<tr><td></td><td>(b)</td><td colspan="2"> 
</td><td>B1 resistor on top of photodiode
B1 photodiode reversed biased</td><td></td></tr>
<tr><td></td><td>(c)</td><td colspan="2">Allows the voltage level to be adjusted.</td><td>B1</td><td></td></tr>
<tr><td></td><td>(d)</td><td colspan="2"><table>
<tr><th>Position of product on belt</th><th>S</th><th>R</th><th>Q</th><th>$\bar{Q}$</th></tr>
<tr><td>before infrared sensor 1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>at infrared sensor 1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>between infrared sensor 1 and 2</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>at infrared sensor 2</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>after infrared sensor 2</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
</table></td><td>B1 for each row</td><td></td></tr>
<tr><td></td><td>(e)</td><td colspan="2">Q changes from 1 to 0 only when infrared sensor 2 is blocked.</td><td>B1</td><td></td></tr>
</table>

	(f)				B1 for Q to Pin 1 B1 for Pin 7 to Pin 13	
	(g)	**(i)**	1001 1001		B1	
		(ii)			B1 Use of correct inputs B1 Correct logic circuit	