Candidate Name ____________________________________

Class	Index Number

ST ANDREW'S SECONDARY SCHOOL
PRELIMINARY EXAMINATION 2024
SECONDARY 4 EXPRESS

ELECTRONICS

PAPER 1 **6063/01**

THURSDAY **15 AUGUST 2024** **2 hours**

INSTRUCTIONS TO CANDIDATES

Do not open this question paper until you are told to do so.

READ THESE INSTRUCTIONS FIRST
Write in dark blue or black pen.
Do not use staples, paper clips, highlighters, glue or correction fluid.

Answer **all** questions from Section A and Section B.

Write your answers to Sections A and B in the spaces provided on the question paper.
You may use a soft pencil for any diagrams, graphs or rough working.

Candidates are reminded that **all** quantitative answers should include appropriate units.
Candidates are advised to show all their working in a clear and orderly manner, as more marks are awarded for sound use of physics than for correct answers.
At the end of the examination, fasten any separate answer paper securely to the Question paper.

FOR EXAMINER'S USE
/ 100

This question paper consists of 23 printed pages.

[**Turn over**

DATASHEET

Resistor Colour Codes

1st Colour Band 1st Digit	2nd Colour Band 2nd Digit	3rd Colour Band Multiplier	4th Colour Band Tolerance
Black 0	Black 0	Black 0	Gold ± 5%
Brown 1	Brown 1	Brown 1	Silver ± 2%
Red 2	Red 2	Red 2	
Orange 3	Orange 3	Orange 3	
Yellow 4	Yellow 4	Yellow 4	
Green 5	Green 5	Green 5	
Blue 6	Blue 6	Blue 6	
Violet 7	Violet 7	Violet 7	
Grey 8	Grey 8	Silver 0.01	
White 9	White 9	Gold 0.1	

Preferred values for resistors (E24 SERIES)

1.0 1.1 1.2 1.3 1.5 1.6 1.8 2.0 2.2 2.4 2.7
3.0 3.3 3.6 3.9 4.3 4.7 5.1 5.6 6.2 6.8 7.5
8.2 9.1 and multiples of ten.

FORMULAE

Astable and monostable generators using 555 timers

Monostable mode Period $T = 1.1RC$

Astable mode Period $T = \dfrac{(R_1 + 2R_2)C}{1.44}$

$t_{on} = 0.7(R_1 + R_2)\,C$

$t_{off} = 0.7\,R_2\,C$

Bipolar junction transistor (BJT)

Current gain, $\beta = \dfrac{\text{Collector current}}{\text{Base current}}$

Voltage gain (for voltage-divider biased CE amplifier, emitter resistor unbypassed)

$\cong -\dfrac{R_C}{R_E}$

Table on Boolean Algebra

Single variable theorems	Laws of Complementation	$0 = 1$ $1 = 0$ $\overline{\overline{A}} = A$
	AND Laws	$A.0 = 0$ $A \cdot 1 = A$ $A \cdot A = A$ $A \cdot \overline{A} = 0$
	OR Laws	$A + 0 = A$ $A + 1 = 1$ $A + A = A$ $A + \overline{A} = 1$
	Commutative Laws	$A + B = B + A$ $A \cdot B = B \cdot A$
	Associative Laws	$A + (B + C) = (A + B) + C = A + B + C$ $A \cdot (B \cdot C) = (A \cdot B) \cdot C = A \cdot B \cdot C$
	Distributive Laws	$A \cdot (B + C) = A \cdot B + A \cdot C$; $(A + B) \cdot (C + D) = A \cdot C + B \cdot C + A \cdot D + B \cdot D$
	Absorptive Laws	$A + A \cdot B = A$ $A \cdot (A + B) = A$ $A + \overline{A} \cdot B = A + B$

Multivariable theorems		$A \cdot (\bar{A} + B) = A \cdot B$
	DeMorgan's Theorems	$(A + B) = A \cdot B$ $(A \cdot B) = A + B$

SECTION A [40 marks]

Answer **all** the questions in the spaces provided.

1 Fill in the missing component name or draw the missing component symbol in the table below. [2]

Component name	Symbol
	
Polarised capacitor	

2 All electronic systems can be broken down into three main system blocks – Input, Process and Output

A list of component units has been provided for you below.

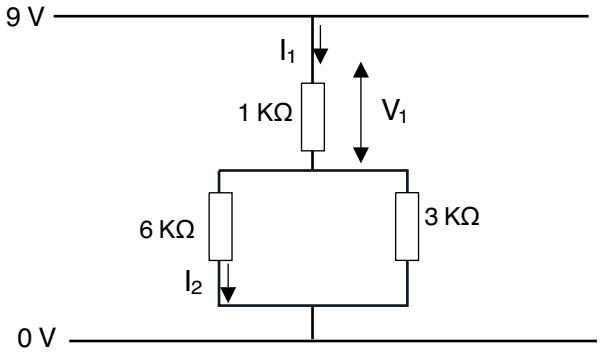
Temperature sensing unit **Motor unit** **SR latch unit**

Moisture sensing unit **OR gate** **Bulb unit**

Write them down under the correct sub-system. The first unit has been placed for you. [5]

Input sub-system	**Process sub-system**	**Output Subsystem**
Moisture sensing unit		

3 A network of resistors is used in the following circuit.



(i) Calculate the resultant resistance of the whole circuit shown.

……[2]

(ii) Determine V_1, the potential difference across the 1 Ωk resistor.

……[2]

(ili) Determine the value of I_1 and I_2.

I_1 =……

I_2 =……
[2]

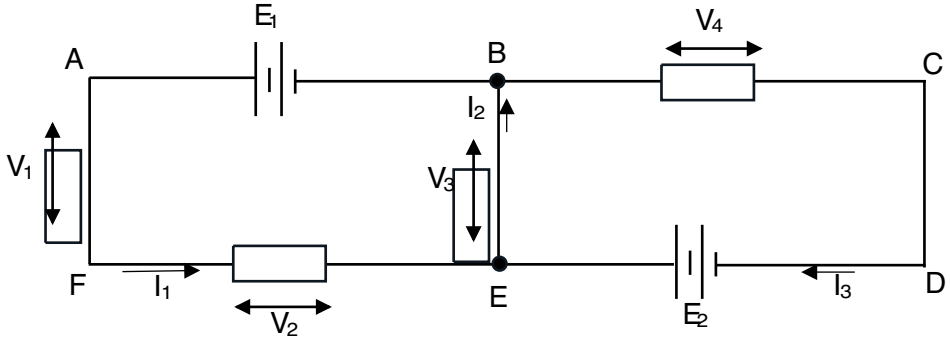
(iv) Determine the energy generated by the 6 kΩ resistor in 6 min.

……[2]

(v) The resistance of the wires has been ignored. Calculate the resistance of the wires given that they are made copper, cross-sectional area = 2 x 10^{-7} m^2, and the total length of the wires used in the circuit is 1.2 m. Resistivity of copper = 1.7 x 10^{-8} Ωm.

……[2]

4 The figure below shows a circuit. The directions of the currents are indicated.



(a) Using KVL, form equations for the loops ABEFA and BCDEB.

ABEFA =.....

BCDEB =.....
[2]

(b) Given E_1 = 12 V, V_2 = 2 V, V_3 = 4 V, E_2 = 5 V, use the equations obtained in (a) to determine V_1 and V_4.

V_1 =.....

V_4 =.....
[2]

(c) Given I_1 = 15 mA and I_3 = 20 mA, determine I_2.

I_2 =.....[1]

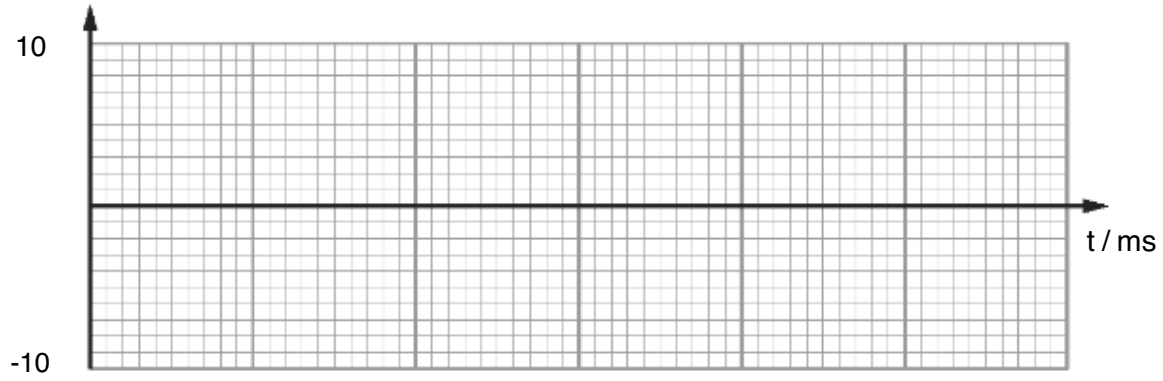
5 A **sinusoidal** waveform has a peak-to-peak value Vpp = 8 V and frequency of 50 Hz.

(a) Determine the period of the wave.

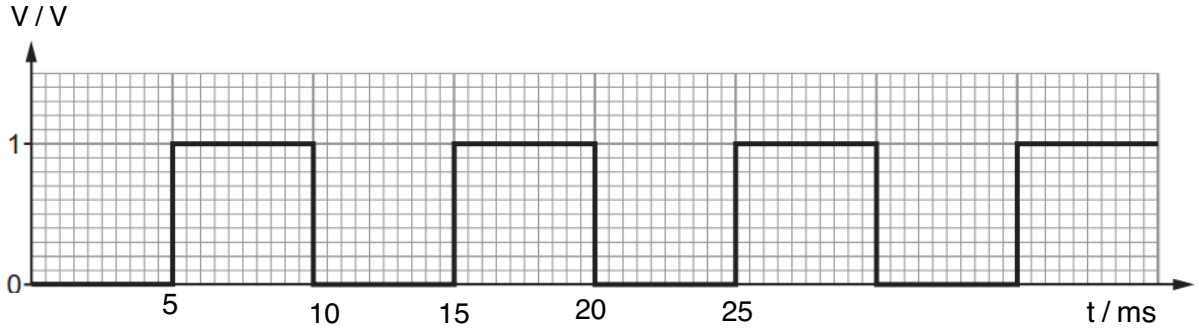
.....[1]

(b) Draw 3 complete waveforms in the graph below. Label the appropriate voltage and time accurately. [2]

V / V



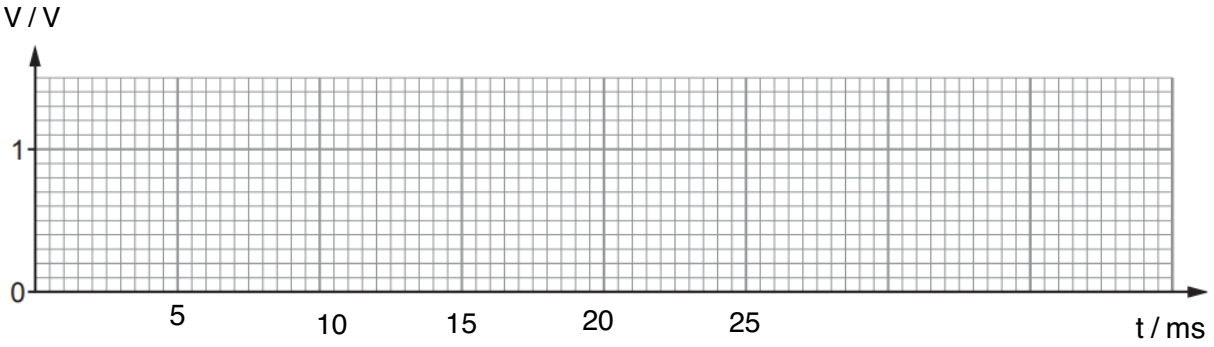
(c) Another waveform is shown below.



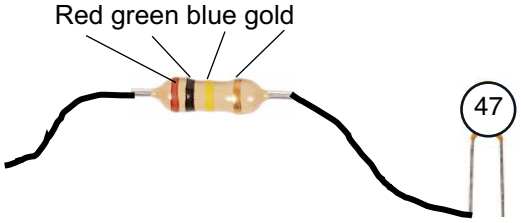
(i) Name the type of waveform shown.

.....[1]

(ii) The signal is then adjusted so that the duty cycle of the waveform is now 70%. Draw the new waveform in the diagram below. [2]



6 An RC circuit is shown below.



(a) Determine the resistance of the resistor.

.....[1]

(b) Determine the capacitance of the non-polarised capacitor.

.....[1]

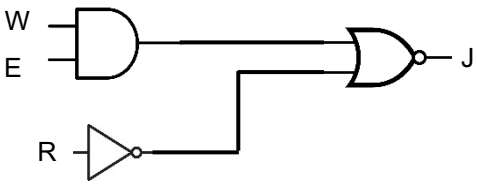
(c) Calculate the time constant of the circuit.

.....[1]

(d) Determine the time taken for the capacitor to be charged to 9 V once the circuit is closed.

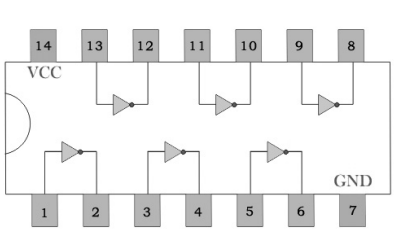
.....[1]

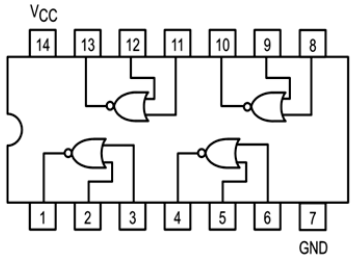
7 A circuit involving a NOT, NOR and AND gate is shown below.

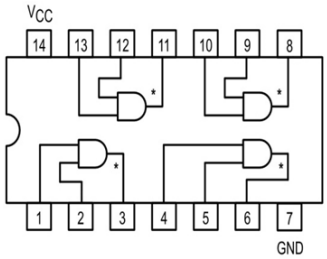


Use a pencil and ruler to draw connections from the three IC chips below to connect the circuit above.

Label your inputs and outputs and **use the gates that are circled**. You may assume that the VCC and GND connections are already made. [3]







8 Convert the following Decimal, Binary and BCD to fill in the blanks in the table below [5]

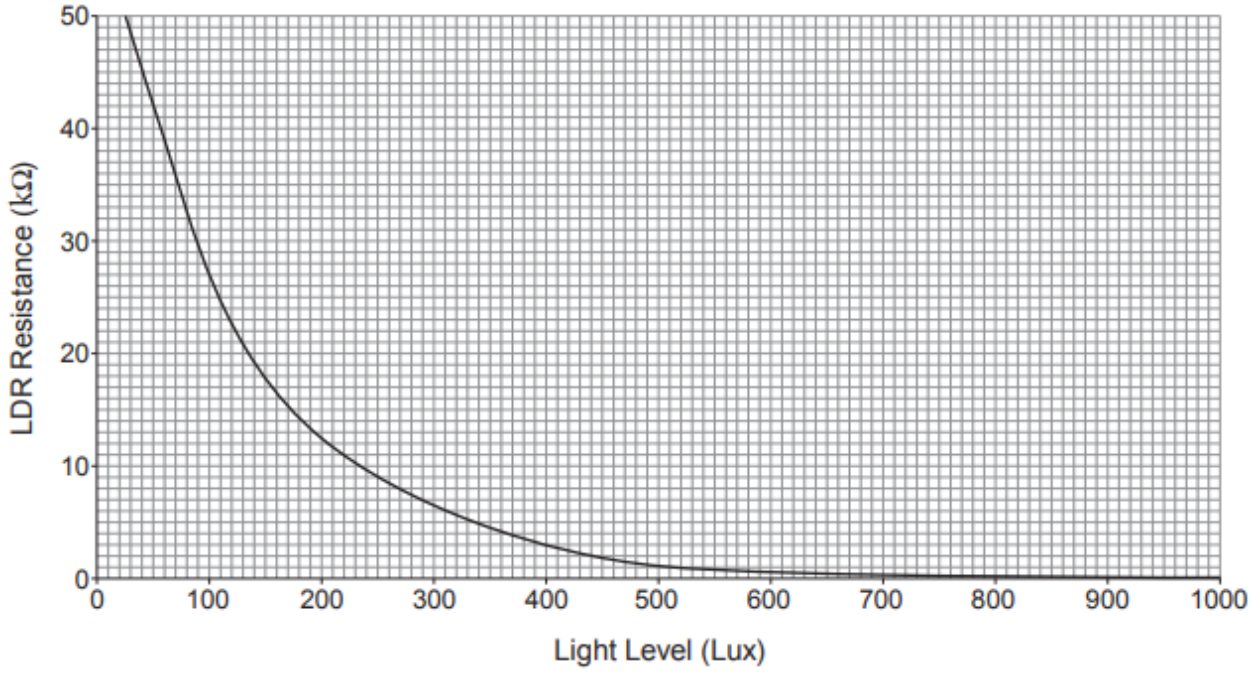
Decimal	Binary	BCD
20	0001 0100	
	11001101	
		0110 0110

SECTION B [60 marks]

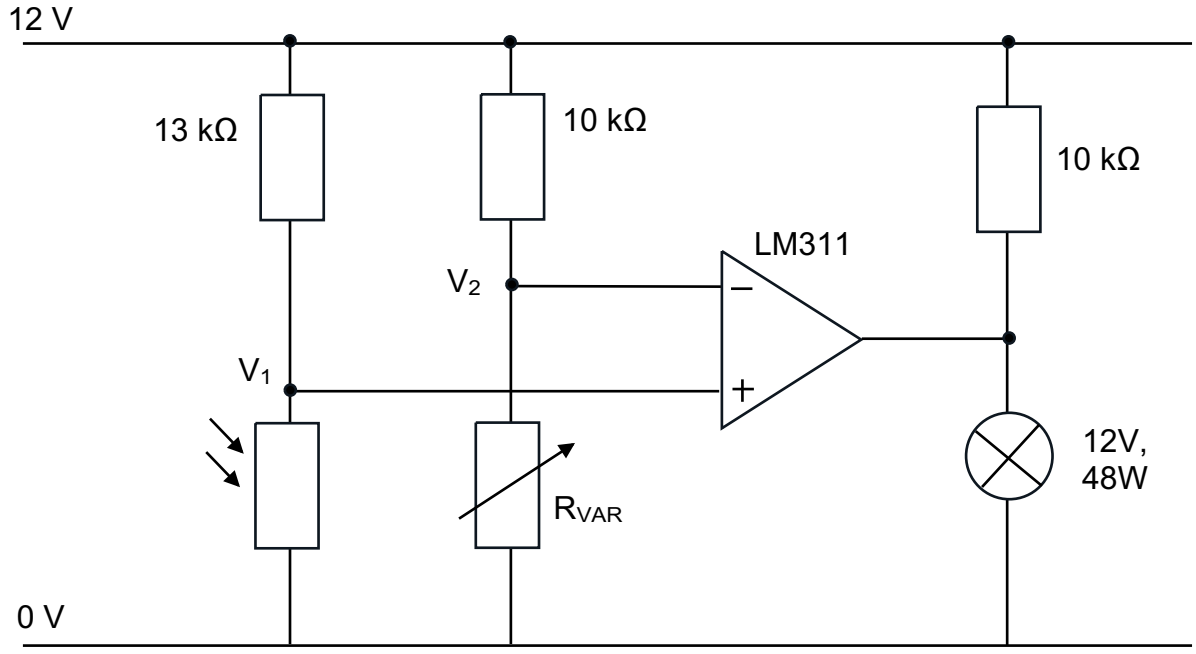
Answer **all** the questions in the spaces provided.

9 **(a)** A student has designed a system to switch on a light in a shop window when it becomes dark.

The characteristic of the LDR used in the design is shown below



The light switches on when the light level drops to 60 lux.



(i) Use the LDR characteristic to determine the resistance of the LDR at 60 lux.

...[1]

(ii) Calculate the value of V_1 at 60 lux

...[1]

(iii) Explain how the circuit turns on the bulb when the light level drops beyond 60 lux.

...

...

...

...[2]

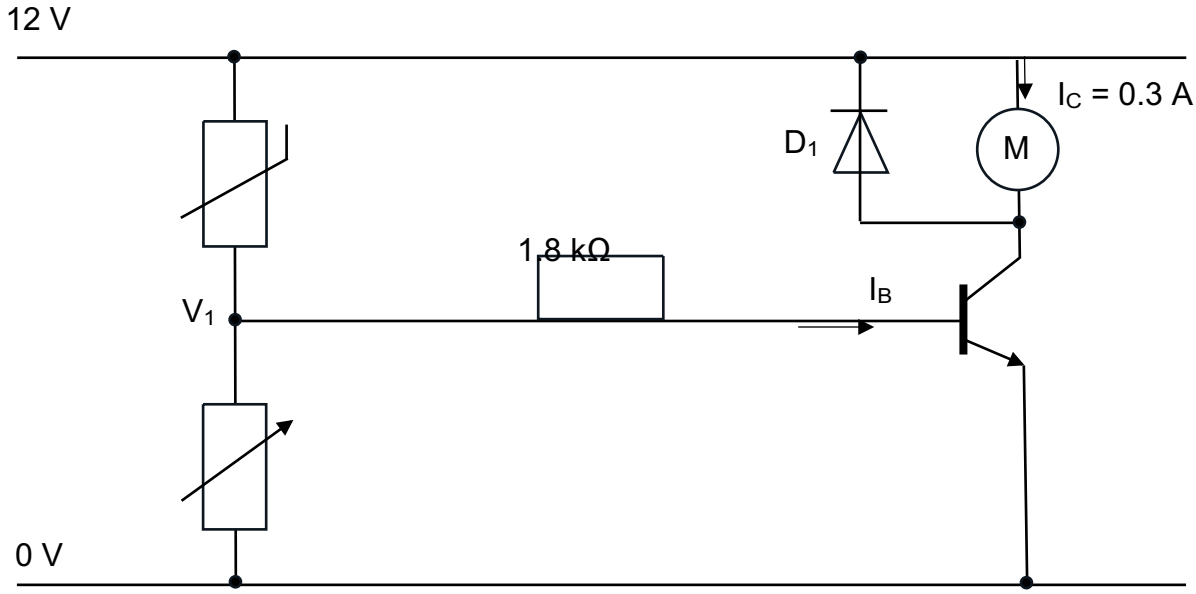
(iv) Calculate the value of the resistance of the variable resistance R_{VAR} for the light to turn on when the light level drops beyond 60 lux.

...[2]

(v) Calculate the current flowing through the light when it is operating at the rated value shown on the circuit diagram.

...[2]

(b) The following diagram shows the circuit for a temperature-controlled fan.



The transistor is just saturated and the current through the fan motor is 0.3A. β = 150, V_{BE} = 0.7 V

(i) When saturated, what is the base current, I_B?

.....[2]

(ii) Thus, calculate the value of V_1 that will ensure that the transistor is just saturated.

.....[2]

(iii) State what component D_1 is and explain its purpose.

.....

.....

.....[2]

(iv) State a reason why transistors are used as switches instead of a mechanical SPST switch.

.....

.....[1]

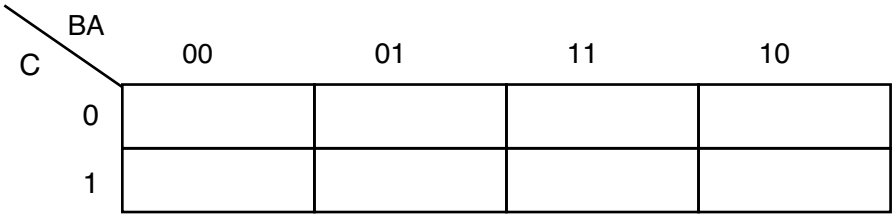
10 A system of logic gates gives the following truth table.

C	B	A	P	Q
0	0	0	0	1
0	0	1	0	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	1	1
1	1	1	0	1

(a) Use the table to write down the un-simplified Boolean expression for output P in terms of C, B and A.

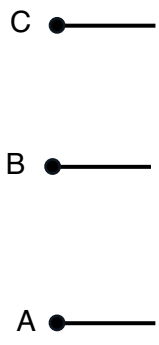
.....[1]

(b) Complete the Karnaugh map and determine the simplest expression for output P.



.....[3]

(c) Draw the logic diagram for P using a combination of NOT, AND and OR gates. [3]



(d) The Boolean expression for Q is

$$Q = \bar{B} + C$$

Show how the output Q can be obtained using only NAND gates. Cross out any redundant gates. [3]

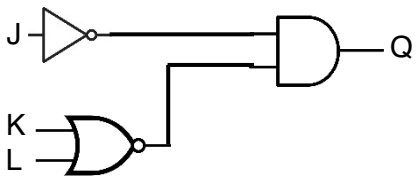
(e) Alfred designed a burglar alarm system to protect his family home.

He placed switches at a window (**W**) and at his front door (**D**). Each switch will output a logic 1 when the window or door is opened. He will have to arm the system using a master switch (**M**). The alarm (**A**) will sound when the master switch is armed and either the window is opened or the door is opened.

Fill in the output for the alarm (A) in the truth table below. [3]

W	D	M	A
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(f) Write down the SOP Boolean expression for the following circuit.



.....[2]

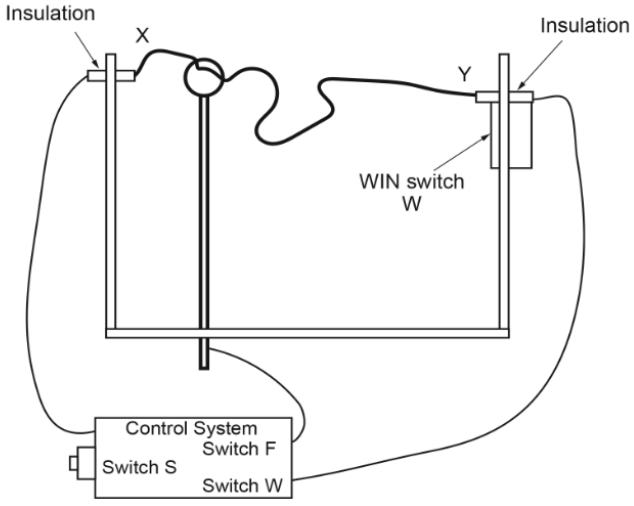
11 A student's design for a "steady-hand" game is shown below.

When the START switch S is pressed the counter starts and the contestant moves the metal loop along the wire from point X to point Y as quickly as possible.

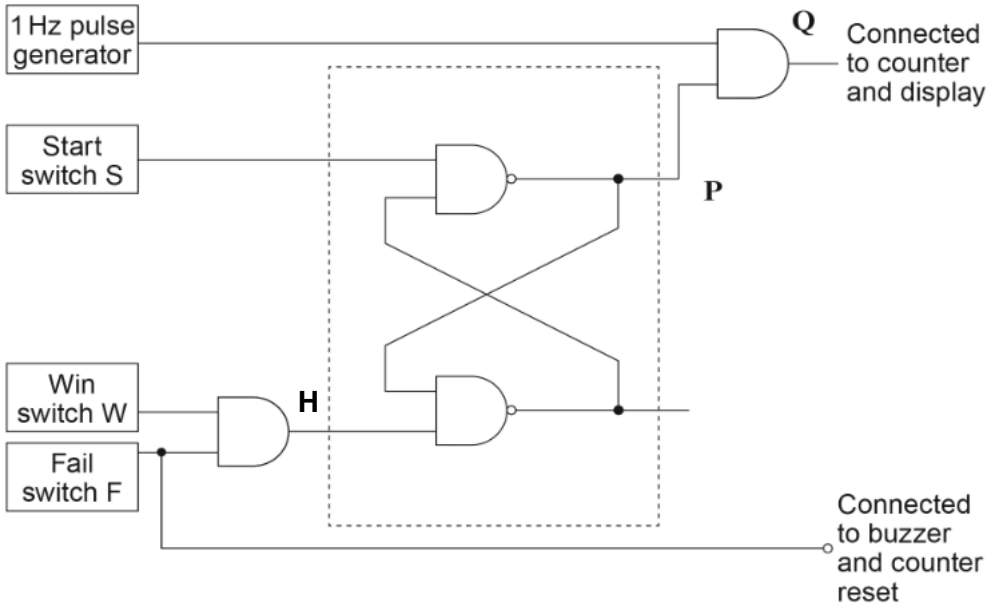
If the metal loop reaches WIN switch W without touching the wire the count shown on the display indicates the time taken.

If the loop touches the wire before the point Y this acts as a FAIL switch F and the counter resets and a buzzer sounds.

Switches S, W and F give a normally HIGH signal until it touches the wire, which will then give a LOW signal.



Part of the control system is shown below.



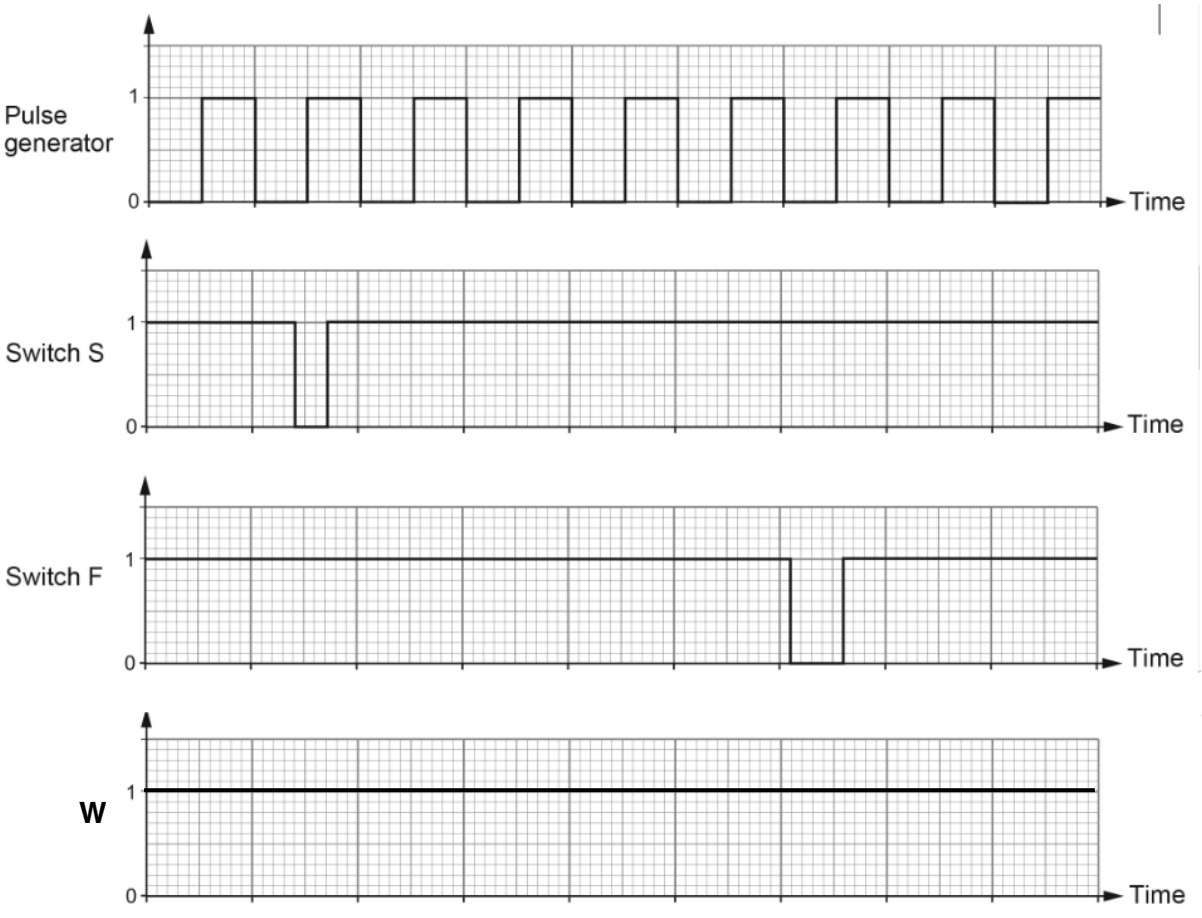
Whilst being attempted, the loop touches the wire part way along. The timing diagram below shows

The output from the pulse generator
The signal from switch S
The signal from switch F

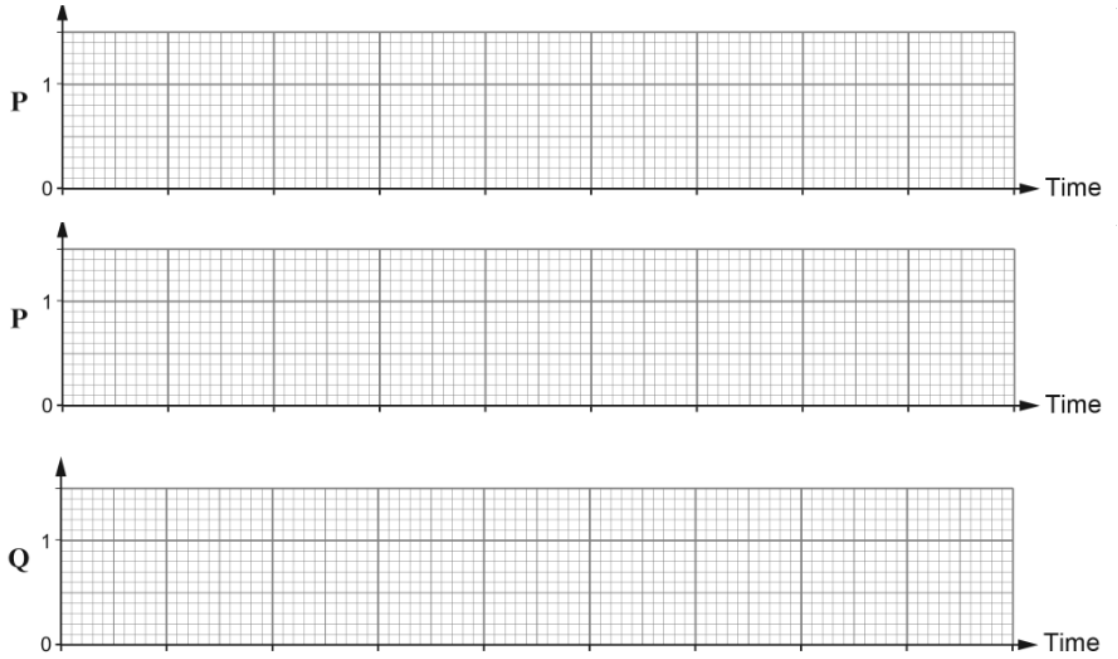
The truth table for the NAND gate SR latch is provided as shown:

S	H	P
1	1	No change
0	1	1
1	0	0
0	0	Invalid state

(a) (i) Complete the diagram to show the outputs H, P and Q. [3]



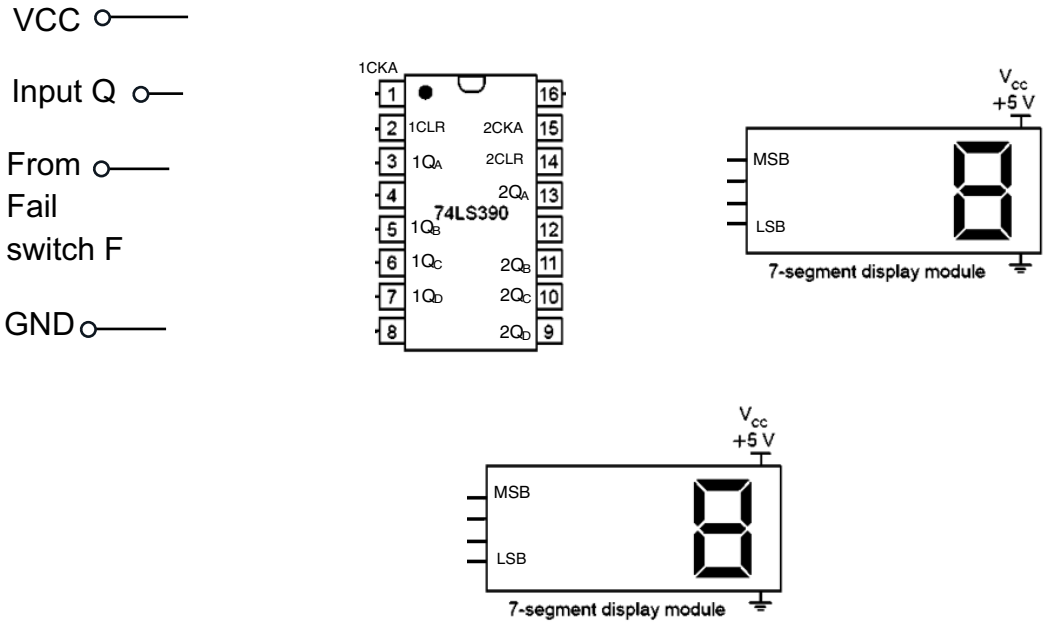
H



(ii) How many pulses will be fed into the counter/display?

……[1]

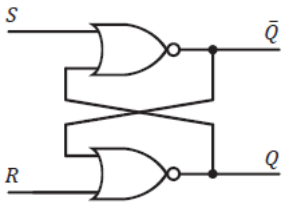
(b) The incomplete counter/display subsystem is shown below.



Complete the circuit diagram so that the display can show a maximum of '99'. Ensure that all pins on the 74LS390 decade

counter is connected. [5]

(c) An NOR gate SR latch can also be used in a variety of applications.

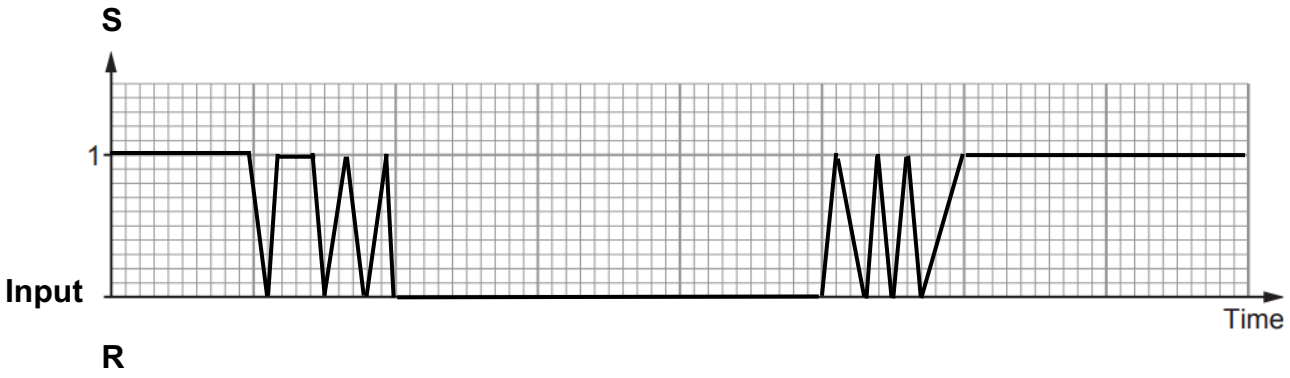


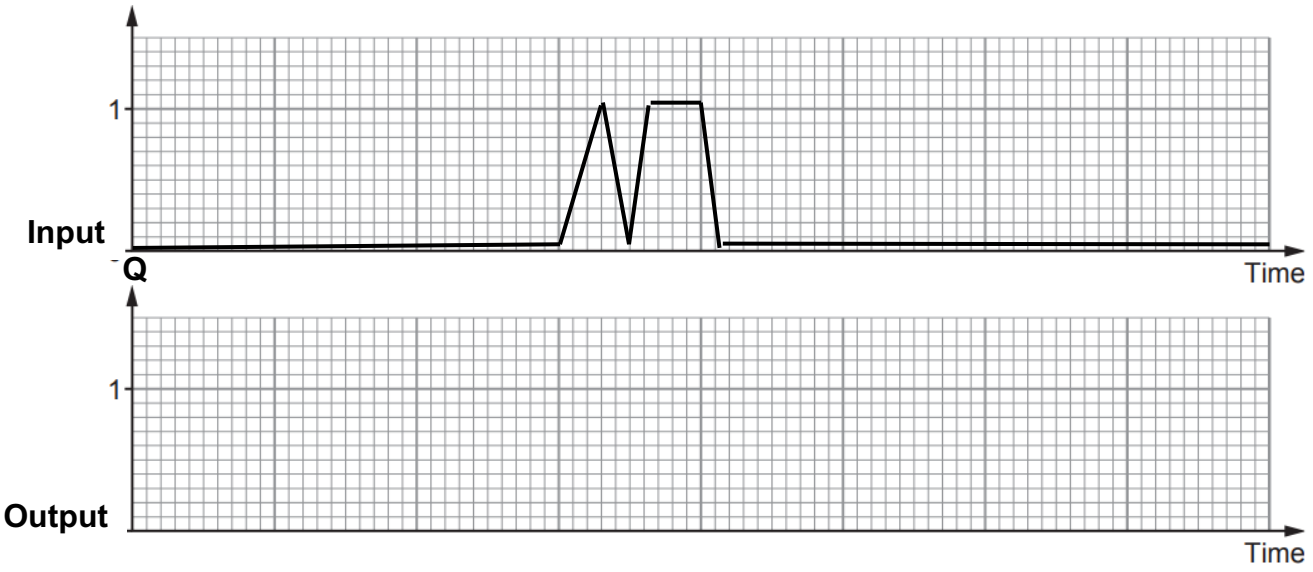
(i) Fill in the truth table for the NOR gate SR latch. [4]

Inputs		**Outputs**	
S	**R**	**Q**	$\bar{Q}$
0	0		
0	1		
1	0		
1	1		

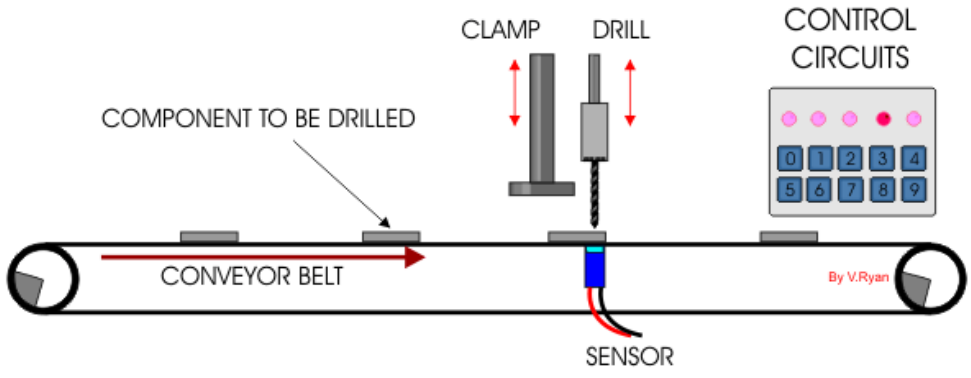
(ii) One of the functions of a NOR SR latch is to debounce a signal.

The diagram below show two signals from a SPDT mechanical switch that is connected to the S and R input. These signals are fed into a NOR SR latch which is used to debounce the S and R signals. Draw the debounced signal (output Q). [2]

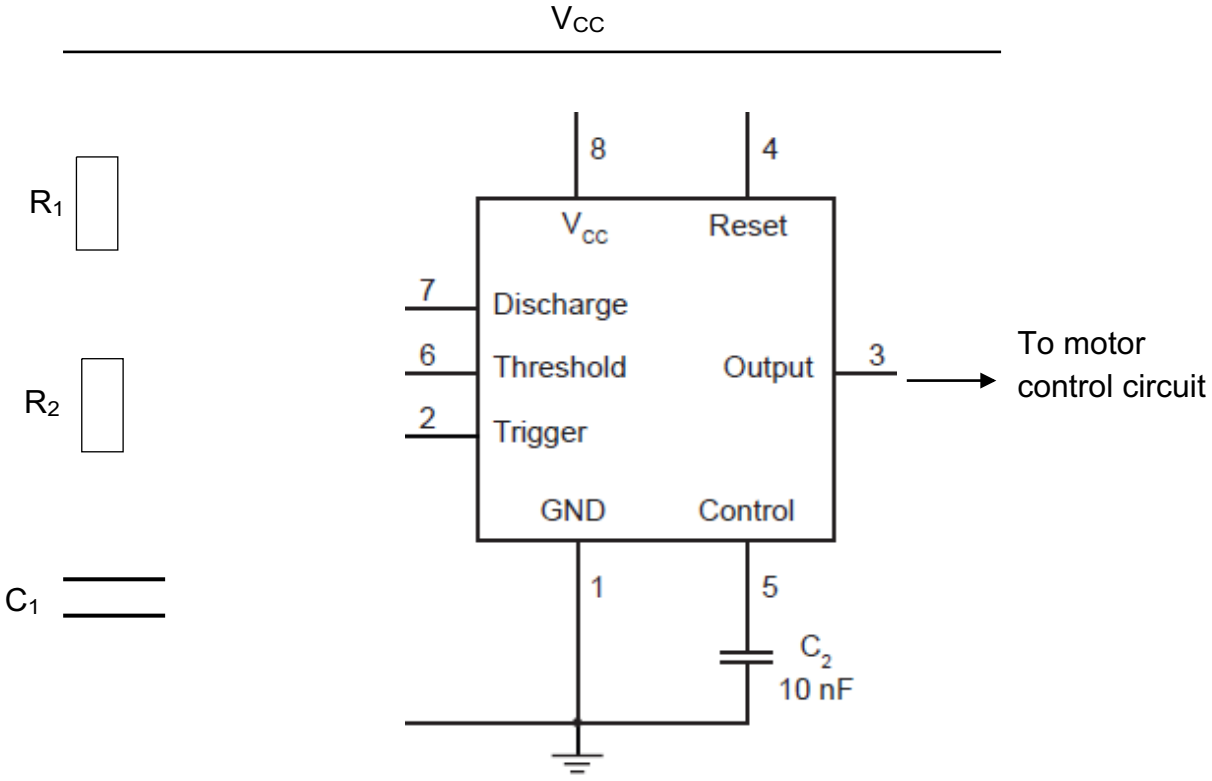




12 The following question is based on the 555 astable circuit. The circuit shown is part of a production line and controls the timing sequence. The automated production line is shown below. Parts / components move along the production line where they are sensed, clamped down, drilled and then released, moving down the production line again. The 555 astable circuit controls the timing of the entire production line.



(a) The timer circuit is found inside the control circuit box. The incomplete circuit diagram is found below. Complete the circuit diagram so that the output is an **astable** signal. Ensure that pins 2, 4, 6, 7 and 8 are connected. [6]



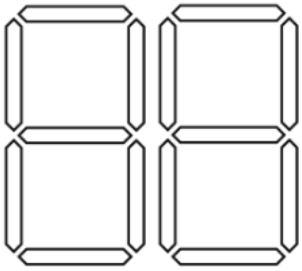
(b) Given that C1 = 47 uF, R_1 = 10 kΩ, choose the resistor value for R_2 so that the frequency of the drill bit motion is 2 Hz.

R_2……[2]

(c) When the system is turned on, a simple message is shown on the control panel, which is made up of two **common cathode** 7- segment displays.

Shade the segments below that light up that show the simple text message when the system is turned on. [2]

DISPLAY A							DISPLAY B						
a	b	c	d	e	f	g	a	b	c	d	e	f	g
0	1	1	0	1	1	1	0	1	1	0	0	0	0



A **B**

(d) The motor is a transducer.

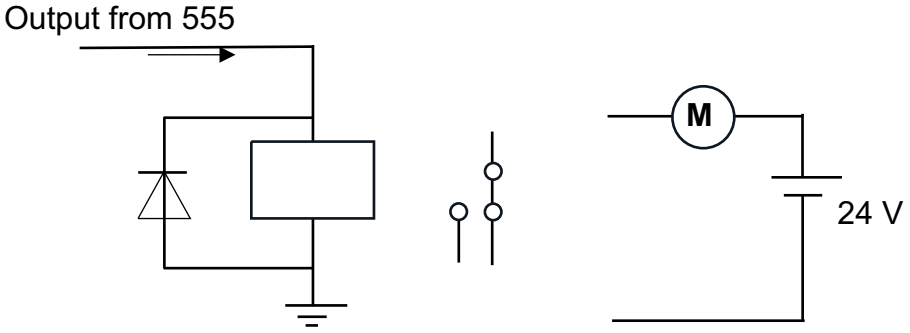
State whether it is an input or output transducer and explain what a transducer is.

.....

.....

.....[2]

(e) The output from the 555 astable is connected to a relay as shown in the circuit below. The motor should only turn on when the output from the 555 is HIGH.



(i) Complete the circuit shown above. [2]

(ii) Explain the purpose of the relay.

...

... [1]

END OF PAPER